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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/752,050	12/29/2000	Ravi Subramanian	9824-035-999	8994

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EXAMINER	
BURD, KEVIN MICHAEL	
ART UNIT	**PAPER NUMBER**
2631	

DATE MAILED: 12/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/752,050	SUBRAMANIAN ET AL.	
	Examiner	Art Unit	
	Kevin M. Burd	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *12/2004*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This office action, in response to the after final amendment filed 8/19/2004, is a non-final office action.

2. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Response to Arguments

3. Applicant's arguments, see the after final amendment filed 8/19/2004, with respect to the rejections of claims 1 and 3-22. Therefore, the rejection has been withdrawn. However, upon further consideration, new grounds of rejection are made in view of the previously used prior art and Selvidge et al (US 5,649,176) and Ott (US 6,400,728).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3-8, 10-12, 14, 15, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dao et al (US 6,275,891) in view of Lowe et al (US 6,173,243) further in view of Selvidge et al (US 5,649,176).

Regarding claims 1, 6 and 10, Dao discloses the signal processing apparatus in figure 1. This circuitry is modified to provide an additional hardware accelerator (channel pooling signal processor) to carry out specific algorithms (column 1, lines 61-63). The hardware accelerator is coupled to the DSP 109 (column 1, lines 64-66) and the DSP performs less computationally intensive tasks than the hardware accelerator (column 1, line 66 to column 2, line 3). Examples of computationally intensive tasks are various coding and compression algorithms, filtering operations and data transforms (column 1, lines 29-32). The hardware accelerator includes a memory (column 2, lines 4-5), means for controlling direct memory transfers to move data across bus 112 (column 2, lines 5-6), additional memories (column 2, lines 13-19), additional busses (column 2, lines 13-19) and interfaces between the hardware accelerator and the DSP (column 2, lines 13-19). All of these elements are computation units and these units direct the transfer of data over the bus 112 (column 2, lines 4-6). This data transfer is the managing of data flow into and out of the channel pooling signal processor.

Dao does not disclose a test interface for testing the function of the plurality of computation units. Lowe discloses it is important to provide means for testing the proper functionality of the system and to provide fault corrections during system operations (column 1, lines 19-32). It would have been obvious for one of ordinary skill in the art at the time of the invention to incorporate the testing method and components of Lowe in the apparatus of Dao. This will increase the reliability and efficiency of any computer system by minimizing or preventing the occurrences of faulty operations (column 1, lines 19-22).

The combination of Dao and Lowe does not expressly state the hardware accelerator is reconfigurable. Selvidge discloses "reconfiguable logic devices also find application as hardware accelerators" as stated in column 1, lines 41-50. It would have been obvious for one of ordinary skill in the art at the time of the invention to utilize the reconfigurable hardware accelerator of Selvidge in the communication system of the combination of Dao and Lowe so the configurable logic devices can easily be configured to perform a desired operation or calculation (column 1, lines 6-8).

Regarding claim 7, Dao discloses specific algorithms are carried out (a data sequencer for controlling program execution), a memory buffer (dedicated memory) and configurable logic (the hardware accelerator is digital circuitry) in column 1, line 61 to column 2, line 13.

Regarding claims 3-5 and 8, the combination is capable of receiving multiple data streams as shown in figure 2 of Dao.

Regarding claims 11, 12, 14, 15, 20 and 21, Dao discloses the computation unites of the hardware accelerator will carry out computationally intensive tasks (column 2, lines 1-3). Examples of these tasks are various coding and compression algorithms, filtering operations and data transforms (column 1, lines 29-32).

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dao et al (US 6,275,891) in view of Lowe et al (US 6,173,243) further in view of Selvidge et al (US 5,649,176) further in view of Ott (US 6,400,728).

Regarding claim 9, Dao discloses the signal processing apparatus in figure 1. This circuitry is modified to provide an additional hardware accelerator (channel pooling signal processor) to carry out specific algorithms (column 1, lines 61-63). The hardware accelerator is coupled to the DSP 109 (column 1, lines 64-66) and the DSP performs less computationally intensive tasks than the hardware accelerator (column 1, line 66 to column 2, line 3). Examples of computationally intensive tasks are various coding and compression algorithms, filtering operations and data transforms (column 1, lines 29-32). The hardware accelerator includes a memory (column 2, lines 4-5), means for controlling direct memory transfers to move data across bus 112 (column 2, lines 5-6), additional memories (column 2, lines 13-19), additional busses (column 2, lines 13-19) and interfaces between the hardware accelerator and the DSP (column 2, lines 13-19). All of these elements are computation units and these units direct the transfer of data over the bus 112 (column 2, lines 4-6). This data transfer is the managing of data flow into and out of the channel pooling signal processor.

Dao does not disclose a test interface for testing the function of the plurality of computation units. Lowe discloses it is important to provide means for testing the proper functionality of the system and to provide fault corrections during system operations (column 1, lines 19-32). It would have been obvious for one of ordinary skill in the art at the time of the invention to incorporate the testing method and components of Lowe in the apparatus of Dao. This will increase the reliability and efficiency of any computer system by minimizing or preventing the occurrences of faulty operations (column 1, lines 19-22).

The combination of Dao and Lowe does not expressly state the hardware accelerator is reconfigurable. Selvidge discloses "reconfiguable logic devices also find application as hardware accelerators" as stated in column 1, lines 41-50. It would have been obvious for one of ordinary skill in the art at the time of the invention to utilize the reconfigurable hardware accelerator of Selvidge in the communication system of the combination of Dao and Lowe so the configurable logic devices can easily be configured to perform a desired operation or calculation (column 1, lines 6-8).

The combination does not disclose an antenna for receiving communication signals. Dao says the system is used in digital communication signals (column 1, lines 14-19) but provides no additional information. Ott discloses a system comprising DSPs and hardware accelerators, as described in column 8, lines 56-62, that receives the input information via an antenna (column 8, lines 63-67). It would have been obvious for one of ordinary skill in the art at the time of the invention to receive RF signals as taught by Ott to be processed by the DSPs and hardware accelerators of the combination of Dao, Lowe and Selvidge. This will limit the computationally intensive error correction routines from having to be done in the base station DSPs (column 8, lines 56-62).

Regarding claims 17 and 18, Dao discloses the computation unites of the hardware accelerator will carry out computationally intensive tasks (column 2, lines 1-3). Examples of these tasks are various coding and compression algorithms, filtering operations and data transforms (column 1, lines 29-32).

6. Claims 13, 16 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dao et al (US 6,275,891) in view of Lowe et al (US 6,173,243) further in view of Selvidge et al (US 5,649,176) further in view of Stilp (US 6,097,336).

Regarding claims 13, 16 and 22, the combination of Dao, Lowe and Selvidge discloses the signal processing apparatus and method of using the signal processing apparatus stated above in paragraph 4. The combination does not disclose what type of signals the apparatus receives. Stilp discloses a receiver for supporting numerous protocols such as TDMA and CDMA (column 18, lines 10-28). "There is significant cost advantage to supporting multiple protocols within a single system." (column 18, lines 10-28). For this reason, it would have been obvious for one of ordinary skill in the art at the time of the invention to incorporate the teachings of Stilp into the signal processing apparatus of the combination of Dao, Lowe and Selvidge.

7. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dao et al (US 6,275,891) in view of Lowe et al (US 6,173,243) further in view of Selvidge et al (US 5,649,176) further in view of Ott (US 6,400,728) further in view of Stilp (US 6,097,336).

Regarding claim 19, the combination of Dao, Lowe, Selvidge and Ott discloses the signal processing apparatus and method of using the signal processing apparatus stated above in paragraph 5. The combination does not disclose what type of signals the apparatus receives. Stilp discloses a receiver for supporting numerous protocols such as TDMA and CDMA (column 18, lines 10-28). "There is significant cost

advantage to supporting multiple protocols within a single system." (column 18, lines 10-28). For this reason, it would have been obvious for one of ordinary skill in the art at the time of the invention to incorporate the teachings of Stilp into the signal processing apparatus of the combination of Dao, Lowe, Selvidge and Ott.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin M. Burd whose telephone number is (571) 272-3008. The examiner can normally be reached on Monday - Thursday 9 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kevin M. Burd
12/19/2004

KEVIN BURD
PRIMARY EXAMINER